Binary-coded decimal code (BCD) converter of proper fractions in the binary code of sequential type

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The purpose of the research was to examine the algorithm of converting BCD of proper fractions in the binary code and to implement the converter of multi-bit fraction of sequential type. The converter of sequential type, unlike Raman converter is characterized by homogeneous circuit constructing and, consequently, by simplicity of increasing the bit of convertible digits. We showed that sequential type converter implementation on programmable logic integrated circuits, for example, the company Xilinx, allows to convert 16-bit fraction for ~ 200 ns, 32-bit — 400 ns at 100 MHz clock.

Keywords: *number system, BCD, binary code, converter, proper fraction, EPLD, sequential circuit.*

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