Theoretical model of Ethernet-switch

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The article describes a proposed theoretical model of the switch. The built model is based on the structural features of the frame of Ethernet technology. We considered the operation of a hypothetical switch of any hierarchical level of a topological scheme of constructing transport system of network. The calculated dependences are aimed at determination of probability and mathematical expectation of the time interlocking frames in switches that implement the second level of the reference model ISO/OSI. A connection is established between the magnitude of the switch delay and requirements of buffer memory required of its input and output ports for all topologies of intersection information flows in the transport systems.

Keywords: *computer network, transport system, transit node, switch, blocking, delay, buffer memory.*

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