Features of Boolean functions synthesis automatization

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In article original approach to automatic synthesis of discrete devices in basis of chips is stated. Methodical installations of this approach are based on mathematical and information descriptions of Boolean functions and their structurally functional decomposition. Parallel and consecutive decomposition on complexity (number of subformulas) are characterized by identical quality, but judging by depth the best quality (smaller or equal value) has the first one therefore we apply parallel decomposition possesses to synthesis of schemes. In particular the computing method for finding of estimates of complexity of realization of any Boolean functions in Zhegalkin's basis on the basis of parallel decomposition is offered. These procedures allow to estimate possibility of minimization of transistors number and time of delay of the scheme. For algorithm some special cases which have been also illustrated by examples are considered. On the basis of these "features" additions are made to algorithm. As a result the algorithm became universal.

Keywords: *boolean functions, complexity indicators, minimization, decomposition, functional equations, schemes.*

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