Comparative evaluation of algorithms of translation and construction of combinational converters of binary integers into BCD and BCD to proper fractions in binary code on FPGA

© V.F. Zhirkov, I.D. Maslov

Bauman Moscow State Technical University, Moscow, 105005, Russia

A comparative evaluation of algorithms for converting numbers and hardware implementation of combinational code converters are considered. Universal algorithms for converting numbers from one positional number system to another are presented, which are essential for the hardware implementation of converters that perform the translation.
The offered comparative evaluation of the algorithms transfer binary integers in BCD and BCD to binary proper fractions. It showed that common feature of these algorithms is the composition of arithmetic operations. Generation in the FPGA of Boolean functions of many variables by tabulated converters allows to reduce the number of stages and code converters and along with other high-performance parameters to achieve low latency propagation (~ 35 ÷ 50 ns) and low power consumption.

Keywords: *number system, binary code, binary- coded decimal notation, algorithm, integer number, proper fraction, conversion, converter, combinational circuit.*

Zhirkov V.F. (b. 1934) graduated from Bauman Moscow Higher Technical School in 1960. Ph.D., Assoc. Professor of the Computer Systems and Networks Department at Bauman Moscow State Technical University. Author of more than 60 scientific papers. Specializes in processing of information in measurement technology.

Maslov I.D. (b. 1992) graduated from Bauman Moscow State Technical University in 2013. Bachelor of information technic and technology. Author of three scientific papers. Specializes in corporate systems consulting and digital signal processing.