Building a converters BCD integers in the binary code and binary code of proper fraction in BCD

© V.F. Zhirkov, I.D. Maslov

Bauman Moscow State Technical University, Moscow, 105005, Russia

The binary algorithms translation analysis of proper fractions in binary-coded decimal and binary-coded decimal integers in binary code was held. It was revealed that the rational choice of algorithms of both types of translation was required to perform the same arithmetic operations, all actions must be performed on the binary-decimal numbers in the decimal system. To implement the converters considered codes and numbers are appropriate hardware BCD 8421. At the same time for both types of transfers required to perform the same correction tetrads elementary transducers of the same type. It is shown that the combination of the elementary transducers reduces the number of stages of the combinational circuit multi-bit converters. Simulation of 32-bit binary code converter proper fractions in binary-coded decimal, the scheme is implemented on the FPGA SPARTAN-II, SPARTAN-3, SPARTAN-6 firm Xilinx, showed that the propagation delay is about 35…50 ns.

Keywords: *number system, binary code, binary-coded decimal notation, algorithm, integer number, proper fraction, conversion, converter.*

Zhirkov V.F. (b. 1937) graduated from Bauman Moscow Higher Technical School in 1960. Ph. D., Assoc. Professor of the Computer Systems and Networks Department at Bauman Moscow State Technical University. Author of more than 60 scientific papers. Specializes in the processing of information in measurement technology. e-mail: jirkovvf@bmstu.ru

Maslov I.D. (b. 1992) graduated from Bauman Moscow State Technical University in 2013, Bachelor of Information Technology. Author of more than 60 scientific papers. Specializes in corporate systems consulting and digital signal processing. e-mail: i.maslov@bmstu.ru