## FPGA testing using pipelined error-detecting codes

## © O.M. Brekhov, M.O. Ratnikov

Moscow Aviation Institute (National Research University), Moscow, 125993, Russia

In this article approach to the solution of FPGA testing and research of characteristics at early development stages is offered. Within this approach universal test firmware based on pipelined control codes generators are offered. Test firmware based on CRC are realized — reveals single and multiple faults and Hamming's code — reveals a fault or refusal place.

**Keywords:** FPGA testing, FPGA screening test, FPGA environment test, pipelined function, CRC, self-correcting code, Hamming codes.

**Brekhov O.M.**, Head of Department, Professor at the Moscow Aviation Institute (National Research University). e-mail: obrekhov@mail.ru

**Ratnikov M.O.**, graduate of the Moscow Aviation Institute (National Research University). e-mail: m.o.ratnikov@mail.ru